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THE HARDWARE DESIGN OF A COGNITIVE MODEL DEMONSTRATOR

by

TIEN-REN RICHARD CHENG

AUGUST, 1969

DEPARTMENT OF COMPUTER SCIENCE
UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN · URBANA, ILLINOIS

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1. INTRODUCTION

This study is concerned with the development and design of the hardware portion of a hypothetical cognition system. One to two decades of experience with machine translation of languages and library information retrival have made it abundantly clear that the ultimate solution of these problems cannot be achieved by pure syntactic analysis, rewriting of constitutents and other related techniques. Completely satisfactory mechanical solution of these interhuman information transfer problems requires mechanical devices which form a representation of "meaning" of the communication -- that is, a more or less rudimentary "understanding" of a communication.

There is substantial psychophysical evidence which supports the hypothesis that language is a particular coding of a more fundamental (probably largely non-linguistic) representation of relationships between physical sensations encountered in the environment. This latter representation is frequently called the "cognitive model" or the "world model". The author is thus motivated to explore a possible working model of the cognitive system.

The hypothetical cognitive system is to be able to perceive (without a TV camera or other projection type of viewer) a scene, interpret the implicit meaning and react properly. In other words, the system is able to detect, discriminate, search file, compare the perceived information with the memorized information and decide how to react. Figure 1 is a simplified block diagram of a hypothetical cognitive system.

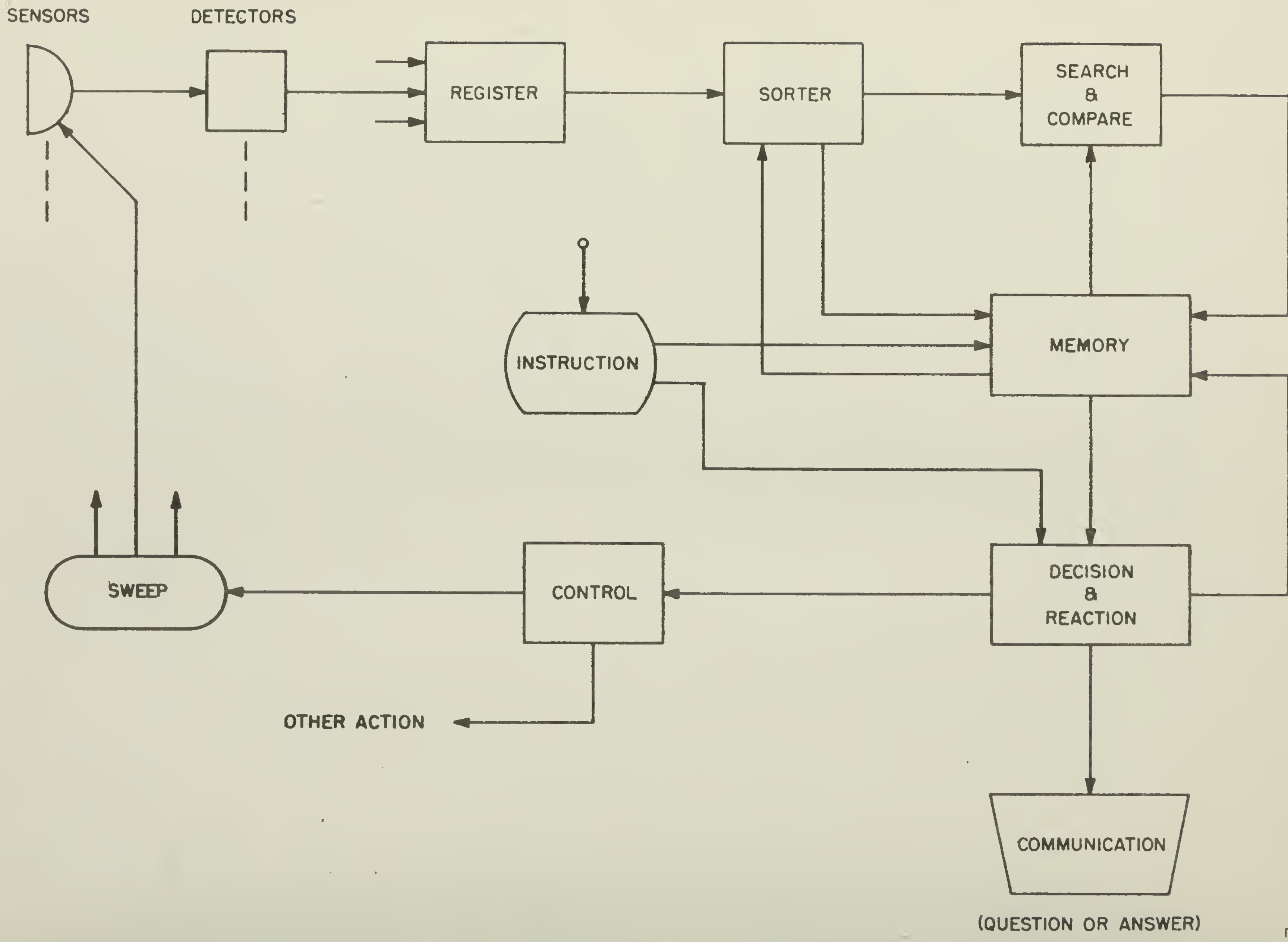

Figure 1. Block Diagram of a Cognitive Model.

The sensor represents a group of various types of devices which respond to various stimuli, e.g. visual, sonic, etc. The detectors detect the information and store it in a temporary storage register. The sorter catagorizes the new information with the assistance of the memory and then the search and comparison system will file the new information at the proper location in the memory and the results from the comparison action are stored in the memory also. A subsystem will decided what reaction should be taken upon the stored information from search and comparison. A communication subsystem will send questions or answers to a human operator by video, audio or other means. If the information being perceived is not complete, the reaction will be to order the sensors to sweep the areas about which more needs to be known. The operator may give instruction to the system by means of keyboard operation or through punched paper tapes.

Although this model can be implemented by hardware alone, large portions of the system can be achieved by software (computer program) representation also. The hardware portion does the detection, encoding and some computation, and then provides the computer with highly pre-processed information.

To study the problems contained in the hardware portion of the overall system, a test model system is designed to demonstrate the basic function. Data obtained will assist further investigation. The model system consists of two major parts: 1) the "front end" of the cognitive system and 2) the scenary representation blocks. The scenary is formed by a group of blocks (e.g. 20 to 30 per scene) placed in a certain arrangement or formation. Each block is to represent a collection of

cognitive information. Thus a group of blocks with significant locational arrangement will represent large amounts of information. From the human observer's view, the blocks are the same size and shape but painted in different colors to identify the attributes. This enables the demonstration of the ability of the front end, i.e. 1) to identify the location of each block and 2) to read the attributes of each block. To demonstrate the information processing ability of the front end of the model, a control system is to react upon the perceived information and rearrange the blocks so the information can be typed out through a teletype console.

2. THE BLOCK DIAGRAMS AND FUNCTIONS OF THE SYSTEM

The hardware portion of the demonstration model of the hypothetical cognitive model consists of two sets of subsystems as indicated in the previous chapter. In this chapter the author intends to introduce the overall system function and then the subsystems. The general function of each subsystem is discussed here and more detailed information is given in Chapters 3 and 4.

2.1 The Overall System

The front end and the blocks are designated as "F" and "B_n". The front end transmits periodically a coded signal which represents the serial numbers of each block. The block responds with the information of its location and the attributes it implements. The front end then codes the attribute information put in the register and then computes the location $P_n(x,y)$ of the block and stores $P_n(x,y)$. The front end then acts upon the second block. All of the coded information in the temporary storage will be sorted and recoded ready for entry into a large scale digital computer. Figure 2 shows the timing of the interaction between front end and the blocks. Figure 3 illustrates the overall system function. The front end transmits the signal with RF modulated infrared, while the block transmits the locational marker in ultra-sonic energy and the attributes in infrared energy.

These modes of transmission are chosen so that an observer will not sense that information has been transmitted from the blocks to the front end. This choice simulates the fact that an observer in a natural

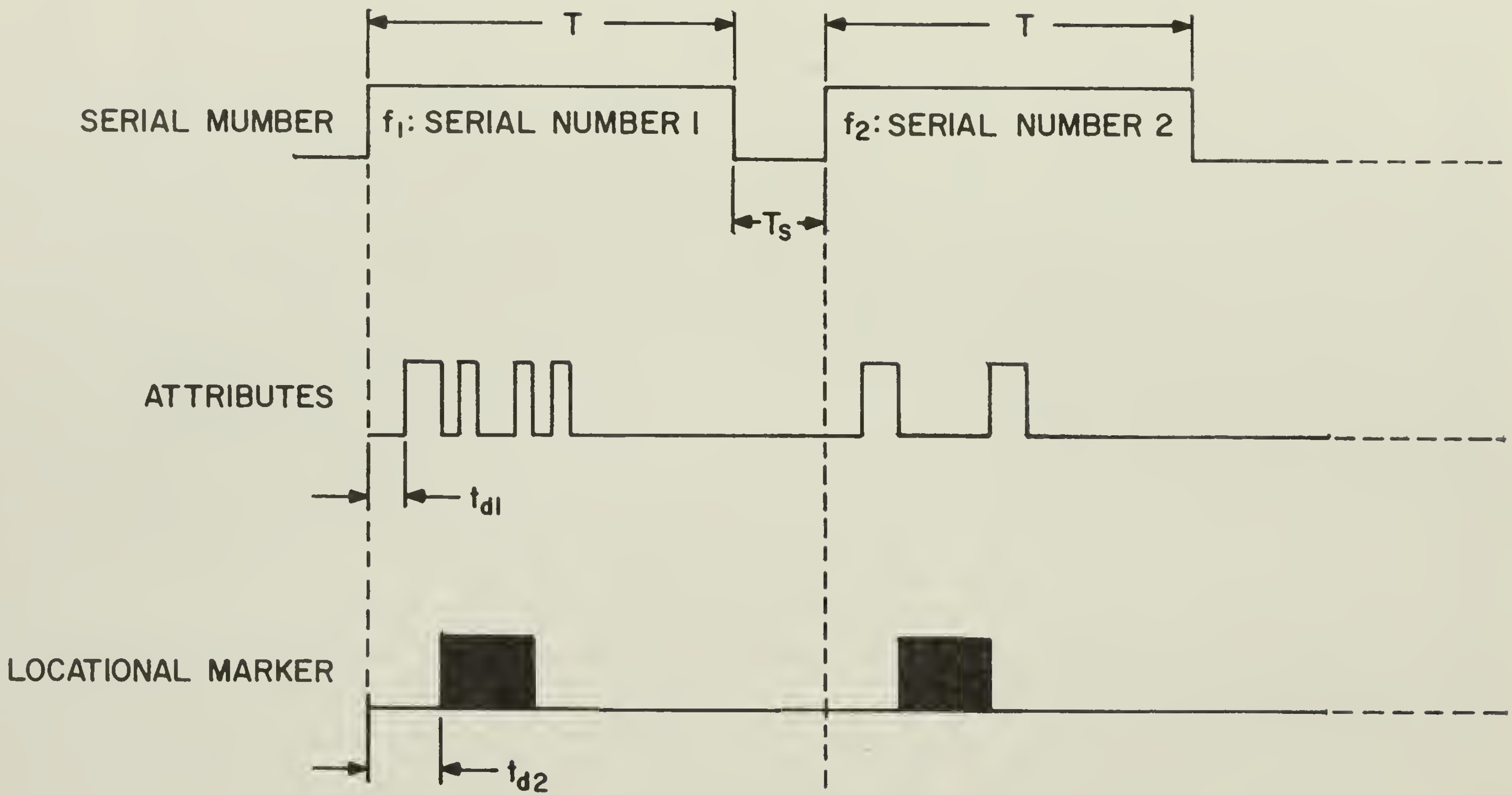

Figure 2. The System Timing Diagram.

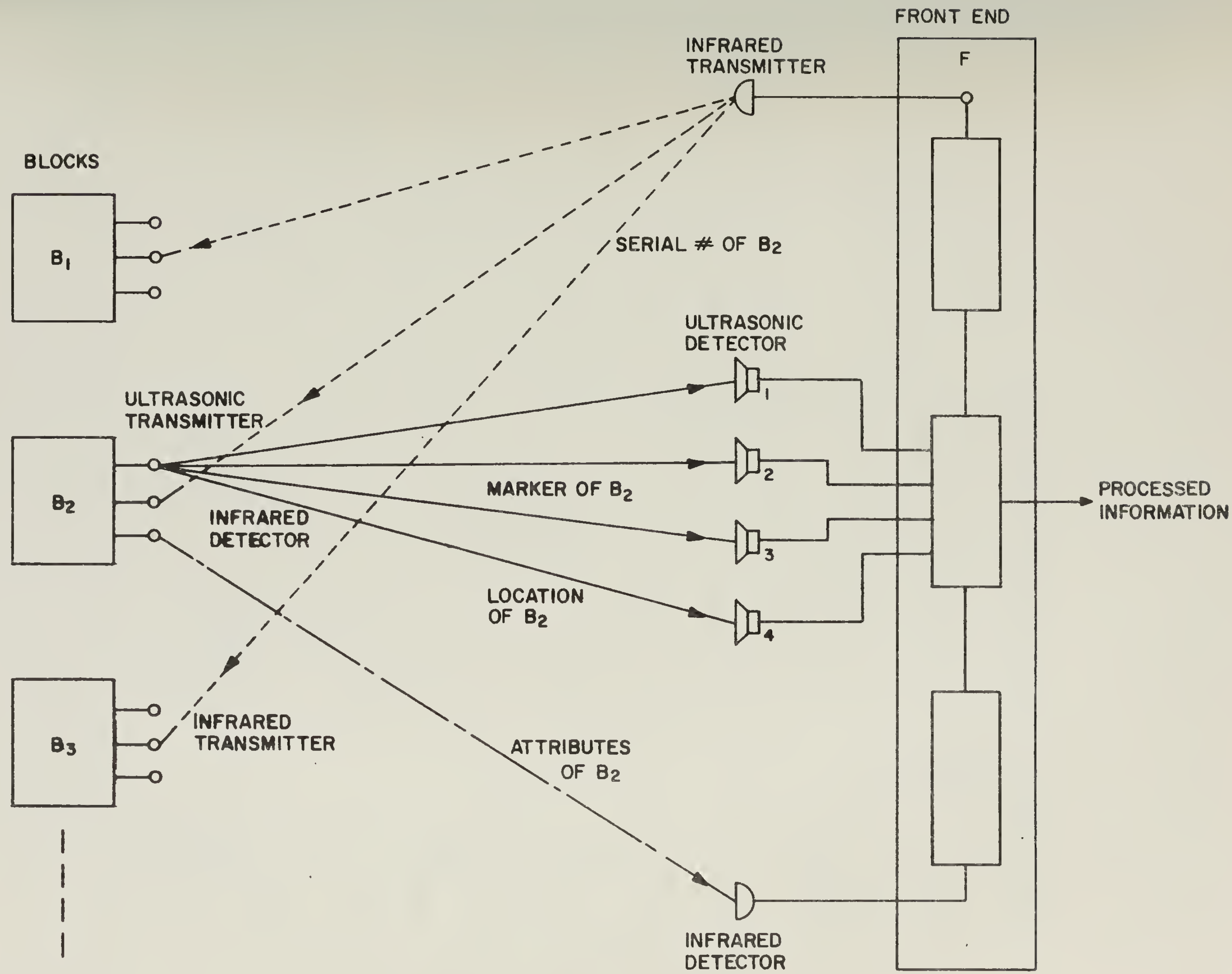

Figure 3. Block Diagram of the Hardware Portion.

situation is unaware that the information has been transmitted in the environment.

2.2 The Functions and Block Diagram of the Block

The block consists of three subsystems: 1) the serial number detector and discriminator; 2) the locational marker generator; and 3) the attributes encoder and transmitter. Figure 4 is the overall block diagram of the complete "block".

The IR detector senses the serial number transmission. If the frequency corresponds to the specific frequency, there will be an output which turns on the trigger generator and generates a pulse "P". "P" triggers monostable multivibrators "A" and "B", where "A" turns on the gate and gates the ultrasonic power into the ultrasonic transducer, "Tus", the transmitter of the locational marker. Since location is computed through time dealy of the ultrasonic signal, the time delay on each component of the system is needed for location computation. Fortunately, the propagation delay in each circuit here is in the range of tens of nano-seconds. The ultrasonic signal is traveling at a speed of around 0.3 meter per millisecond. Thus an average sum of time delay $t_d = t_a + t_b + t_g + t_k + t_m$, as shown in Figure 4, is accurate enough for the computation. Monostable multivibrator "B" is used to gate the pulses to a ring counter. The ring counter distributes the pulse through a digital encoder which codes the attributes of this block. The digital codes are then transmitted by the infrared emitter.

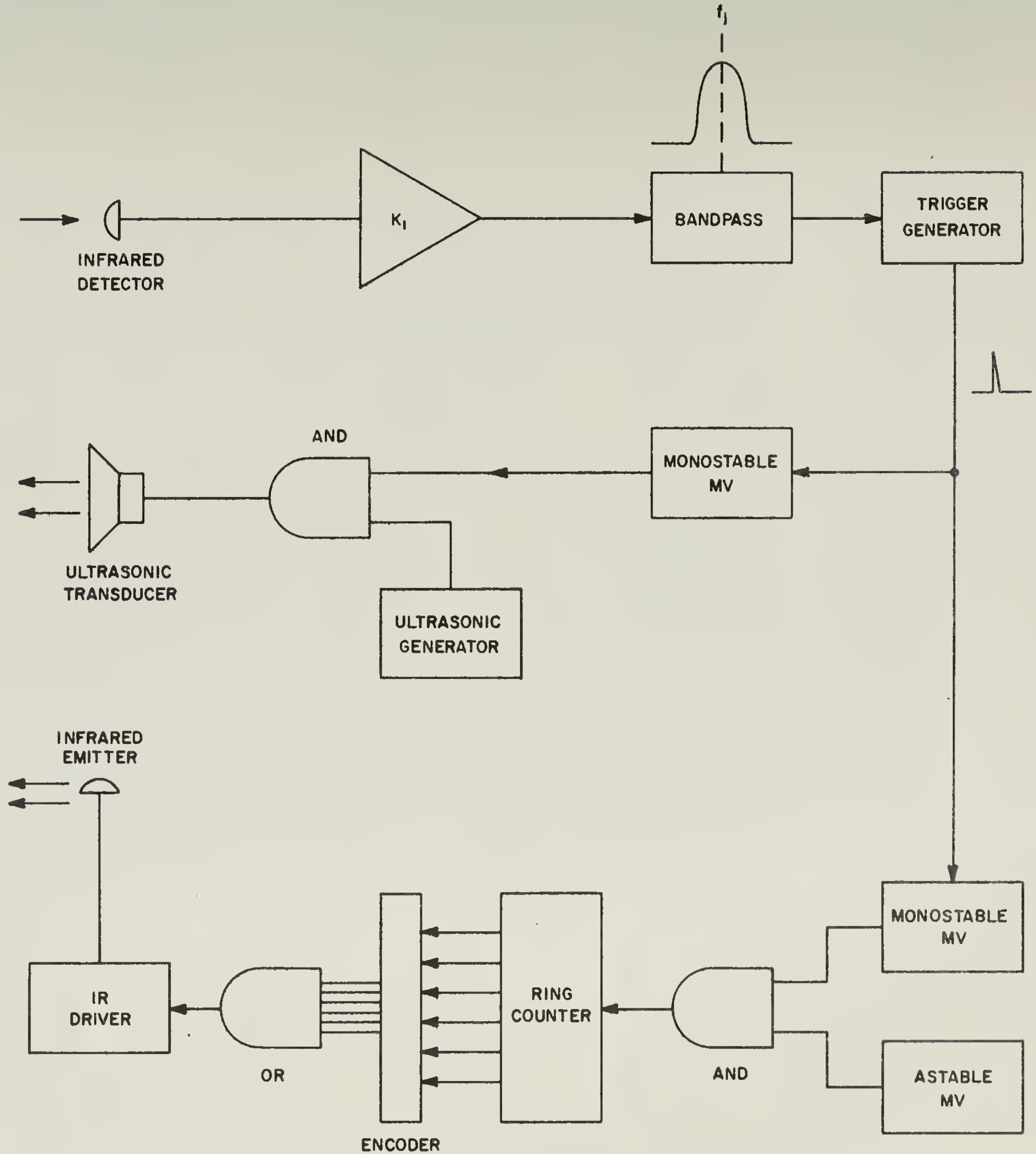

Figure 4. The Block.

2.3 The Functions and Block Diagram of the Front End

The front end consists of five major circuits: 1) the serial number generator and transmitter; 2) the ultrasonic detector and time detector; 3) location computer; 4) the attributes detector; 5) threshold encoder. Due to the complexity of the system and the separability of the circuits, the overall block diagram is shown in Figure 5 in an over-simplified form and some more complicated subsystems will be shown independently.

The clock pulse triggers the serial number generator and the time detector simultaneously. When the ultrasonic detector detects the responding locational markers from a block, a trigger pulse is generated which triggers the time detector to generate a pulse with width T seconds corresponding to the distance between the block and ultrasonic detector. The pulse width is converted into voltage amplitude and together with three other pulses is fed into the locational computer to find the coordinates x and y. The analog P(x,y) signal is digitized and coded through a threshold encoder. Simultaneously, the attribute detector senses the coded pulse and stores it in the register. After the completion of the information processing of a block, the information is fed to computer storage. The second clock pulse repeats the same cycle until the last serial number is addressed. A signal is sent to the computer indicating the completion of this "perception".

Figure 6a shows the locational computation system and Figure 6b illustrates the locational computing subsystem for x coordination.

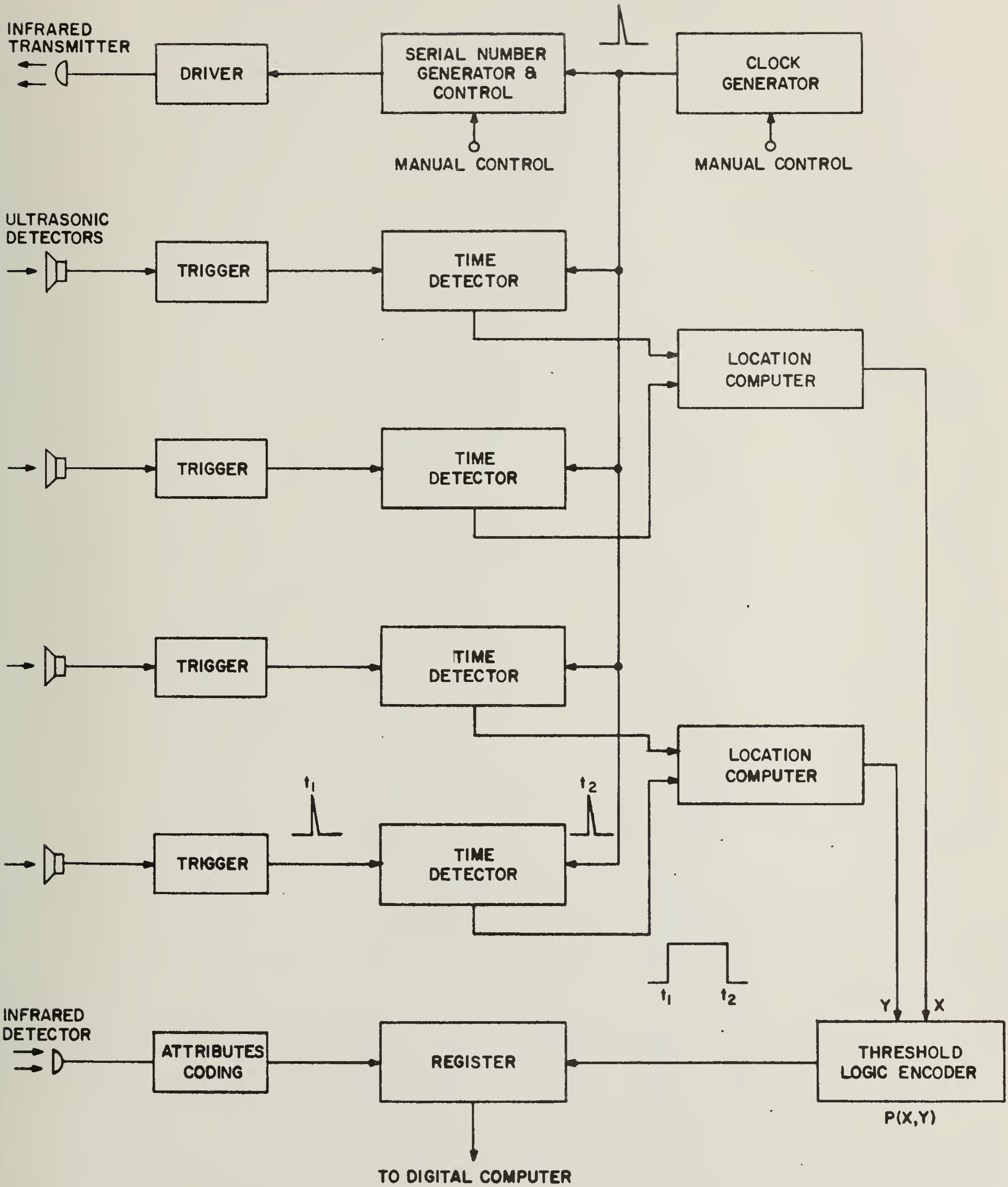

Figure 5. The Overall Block Diagram of the Front End.

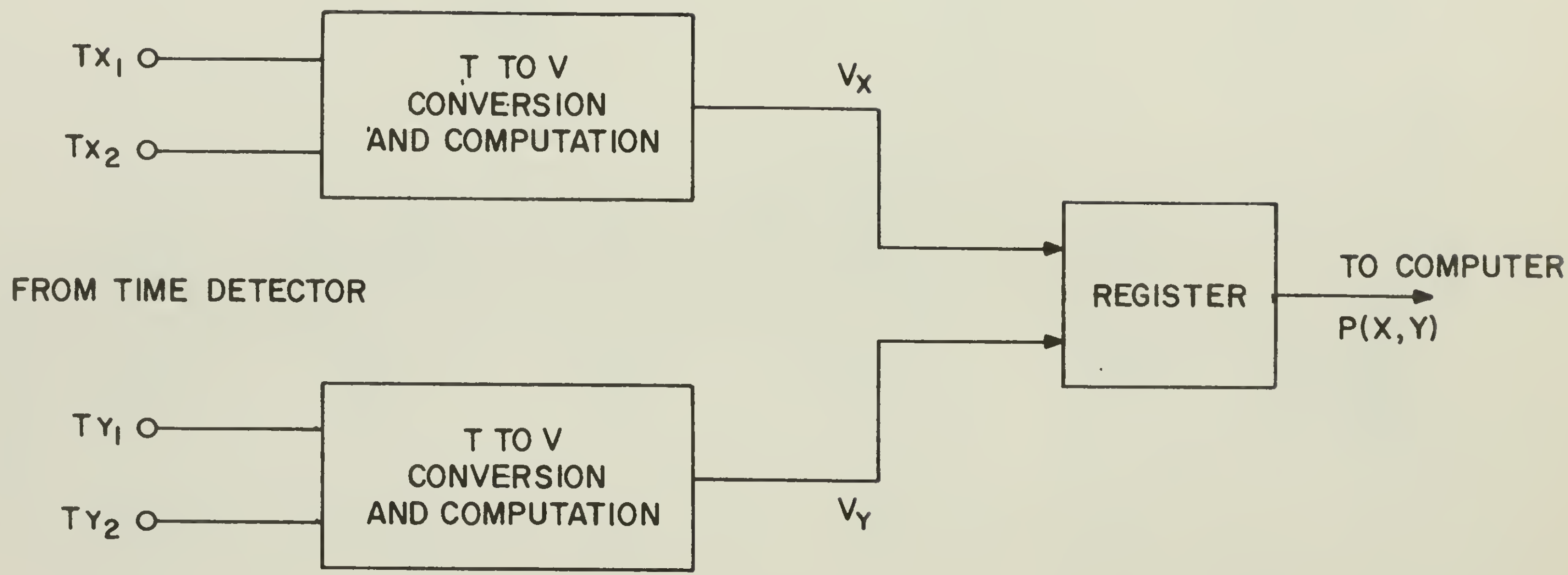

Figure 6a. The Locational Computation System.

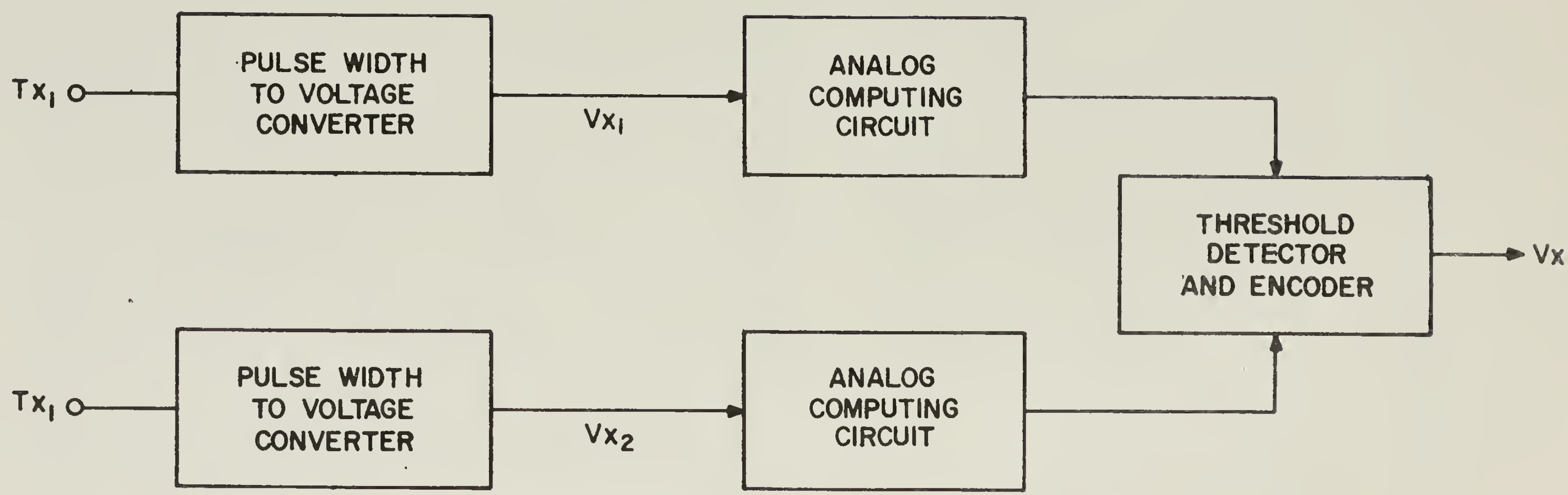

Figure 6b. The Locational Computing Subsystem for x Coordination.

3. THE CIRCUITS AND FUNCTIONS OF THE BLOCK

The Block contains three independent groups of circuits: 1) the serial number detector and trigger generator; 2) the locational marker generator and transmitter; 3) the attributes encoder and transmitter. The block has a size of $4 \times 4 \times 3\ cm^3$ to contain all of the integrated circuits and a transistor. It is powered by two miniature batteries. The author intends to discuss the generally used circuit briefly and only give the detailed discussion to the specially developed circuits for this system.

3.1 The Serial Number Detector and Trigger Circuit

This is an infrared (IR) detection circuit which detects and demodulates the frequency modulated infrared signal. A bandpass filter is used to discriminate the incoming frequencies. If the output of the filter reaches a defined voltage, the trigger circuit will generate a sharp pulse to start the sequential operation of the block.

The IR Detector Circuit is shown in Figure 7. In the quiescent state, i.e. when there is no IR signal, R_3 is adjusted to balance the bridge. A differential amplifier K_1 is used to amplify the signal level for the bandpass filter input. Since the differential amplifier has very high Z_{in}, the IR diode is chosen to have high resistance, thus the detector portion power consumption is minimized.

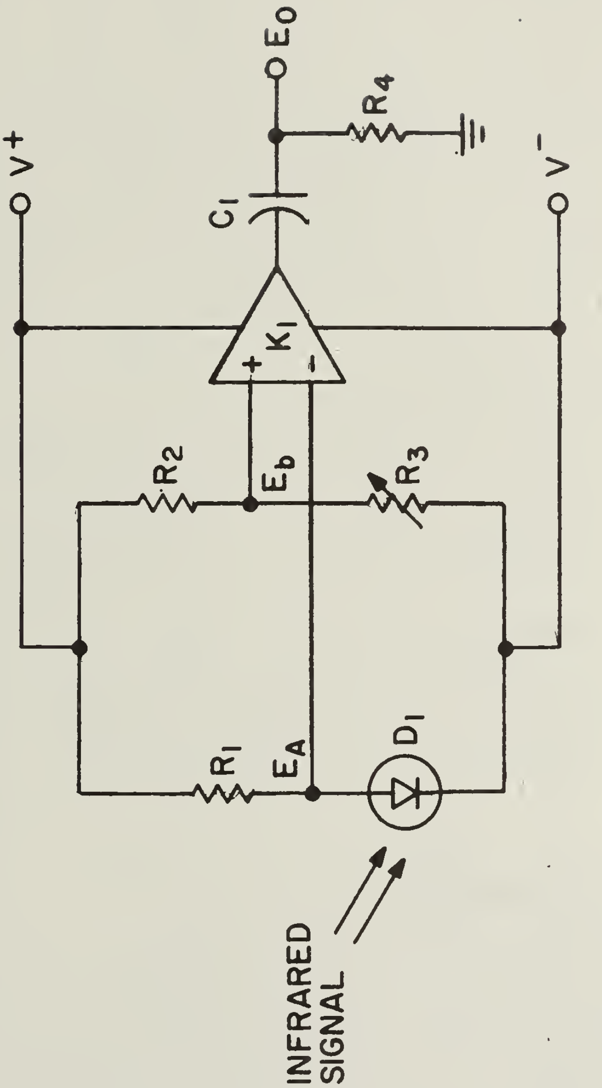

Figure 7. The Serial Number Detector Circuit.

3.2 The Bandpass Filter Circuit

Due to the possible frequency drifts in the frequency generator and in the tuned circuit in the block, each block is assigned a band of frequency instead of a single resonant frequency. Since low frequency RF is used in the system, an LC circuit would be too large to put in the block. An active RC filter is thus designed for this purpose. By using high Z_{in} operational amplifiers the size of the filter is very small. The bandpass filter circuit is shown in Figure 8.

3.3 The Trigger Generator Circuit

The trigger generator produces a sharp pulse upon the output from the bandpass filter. This pulse is to trigger the location mark generator and the attribute encoder. The trigger circuit is shown in Figure 9. It is essentially a Schmitt trigger circuit with D_1 and C_1 to rectify and smooth the filter output. When T_2 is switched off, a positive pulse is emitted from the differentiator, C_2 and R_b.

3.4 The Attributes Encoder

The attributes encoder is shown in Figure 10. It is a programmable digital encoder which produces a serial six bit signal. The signal starts upon the trigger pulse. The coding programmer is a set of six junctions (simulation of switches) programmed by connecting with wires to obtain a "1" and disconnecting the junction to obtain a "0". The pulses are generated by a free running multivibrator and then distributed by a circular counter.

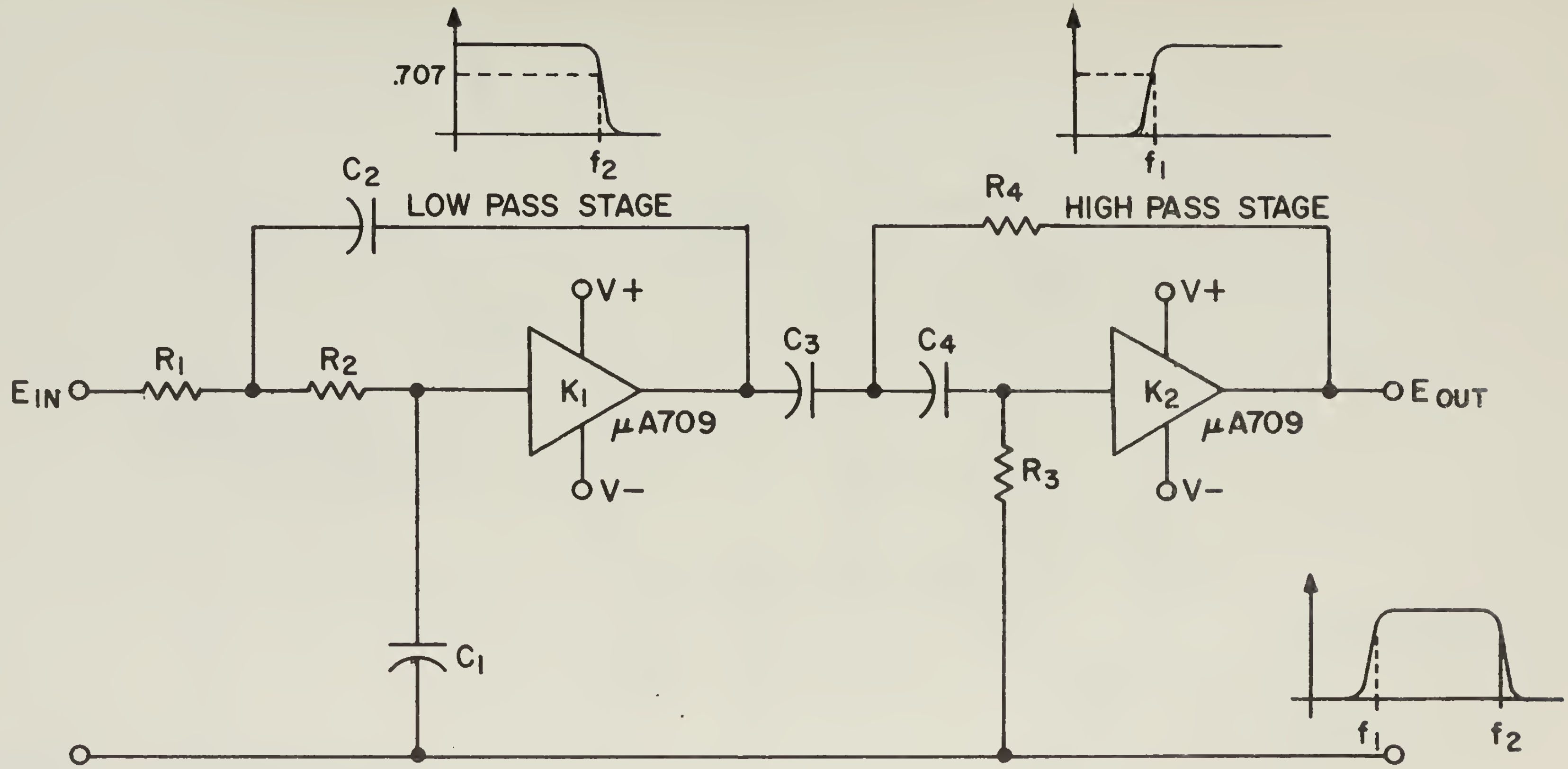

Figure 8. The Bandpass Filter Circuit.

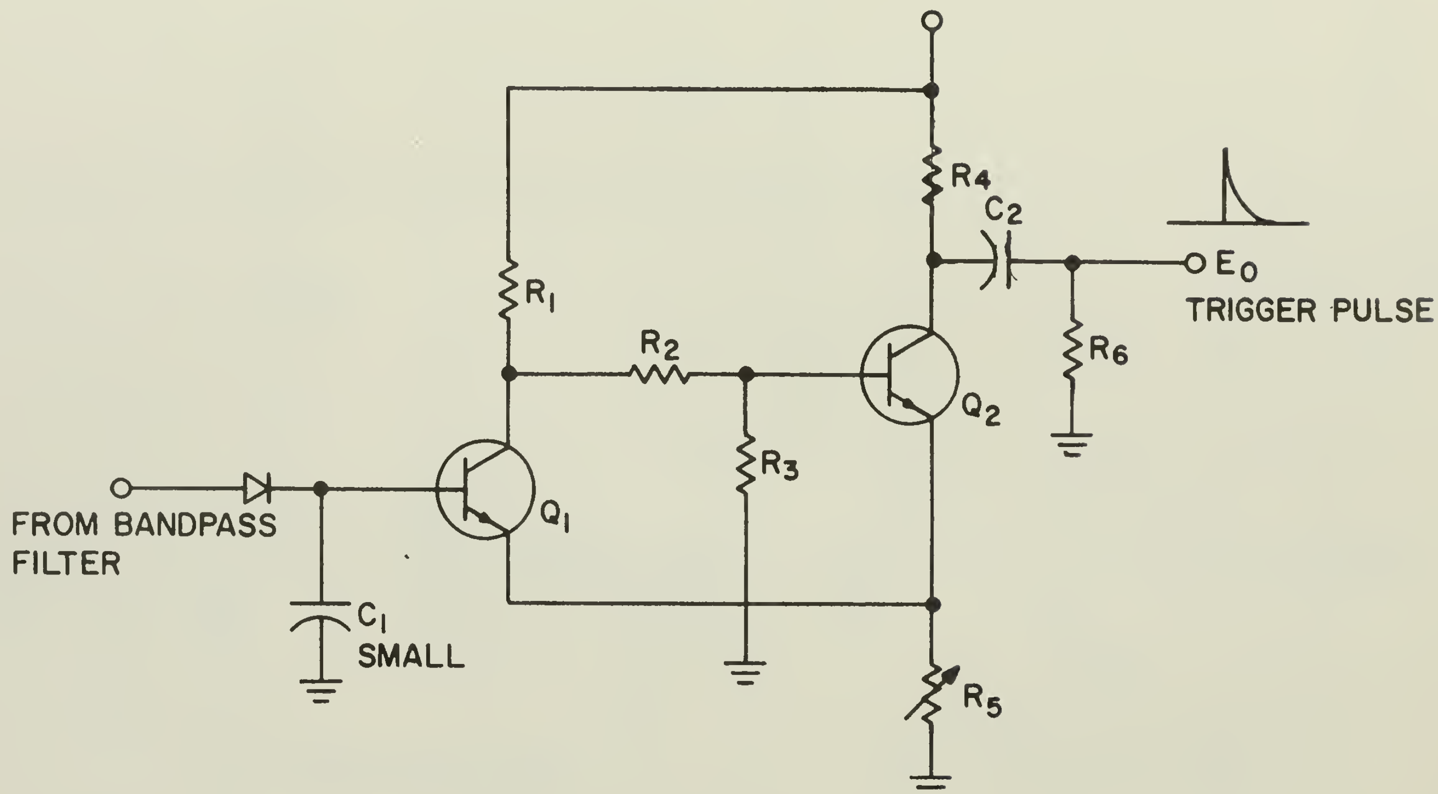

Figure 9. The Trigger Generator.

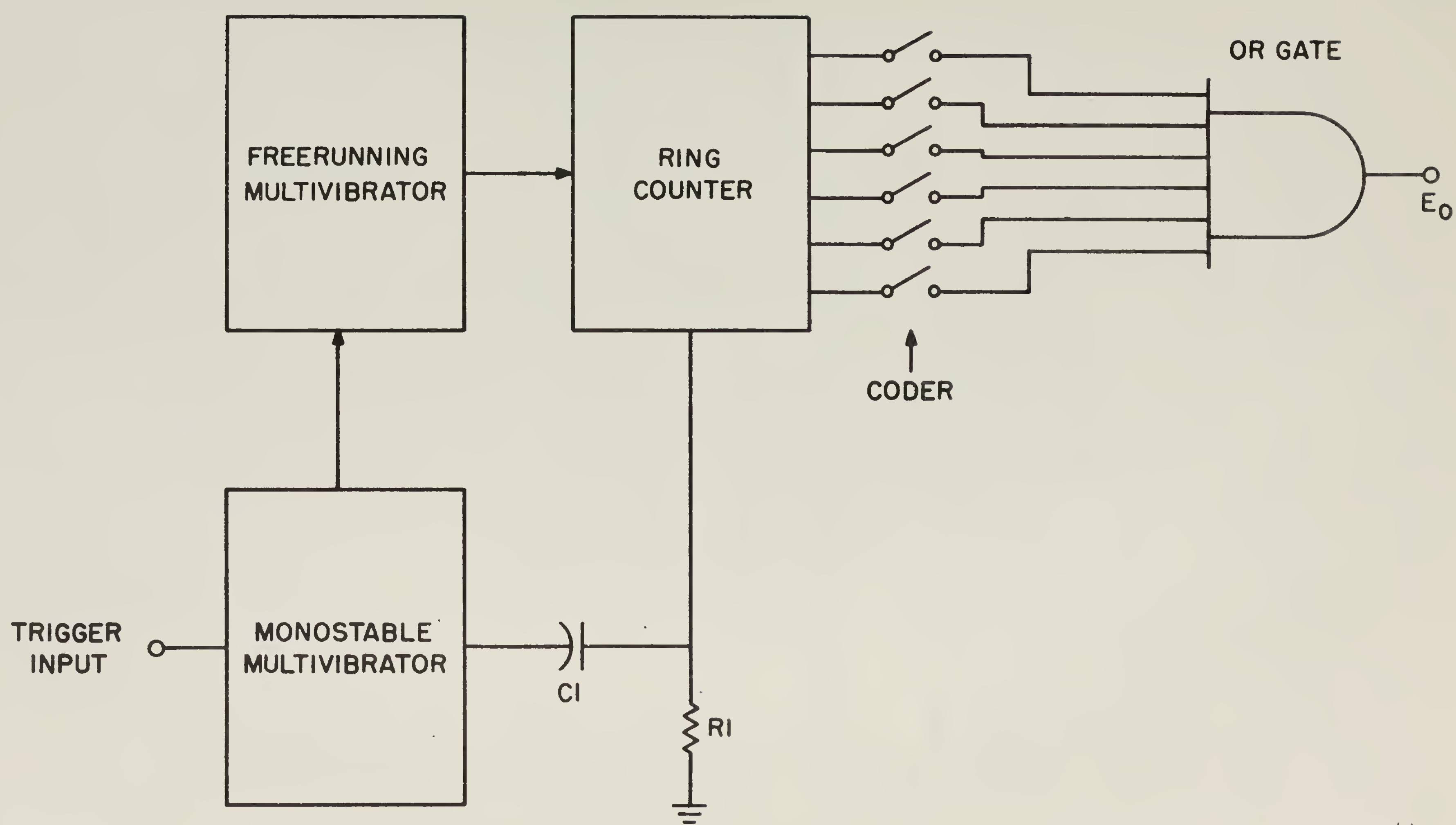

Figure 10. The Attributes Encoder.

If more words are needed to code the attributes, a version of the encoder is shown in Figure 11.

3.5 The Infrared Transmitter

The IR transmitter is an infrared emitting diode which is driven by a transistor amplifier. The amplifier is a single stage emitter follower to match the characteristics of the IR emitting diode. The infrared transmitter is shown in Figure 12.

3.6 The Ultrasonic Locational Marker Generator and Transmitter

The ultrasonic signal is generated by a simple Armstrong oscillator. To insure fast response to the trigger pulse, the oscillator is operating all the time on stand-by. When the circuit is triggered the ultrasonic signal is then gated into the transducer and the length of the transmission is controlled by a monostable multivibrator. The circuit is shown in Figure 13.

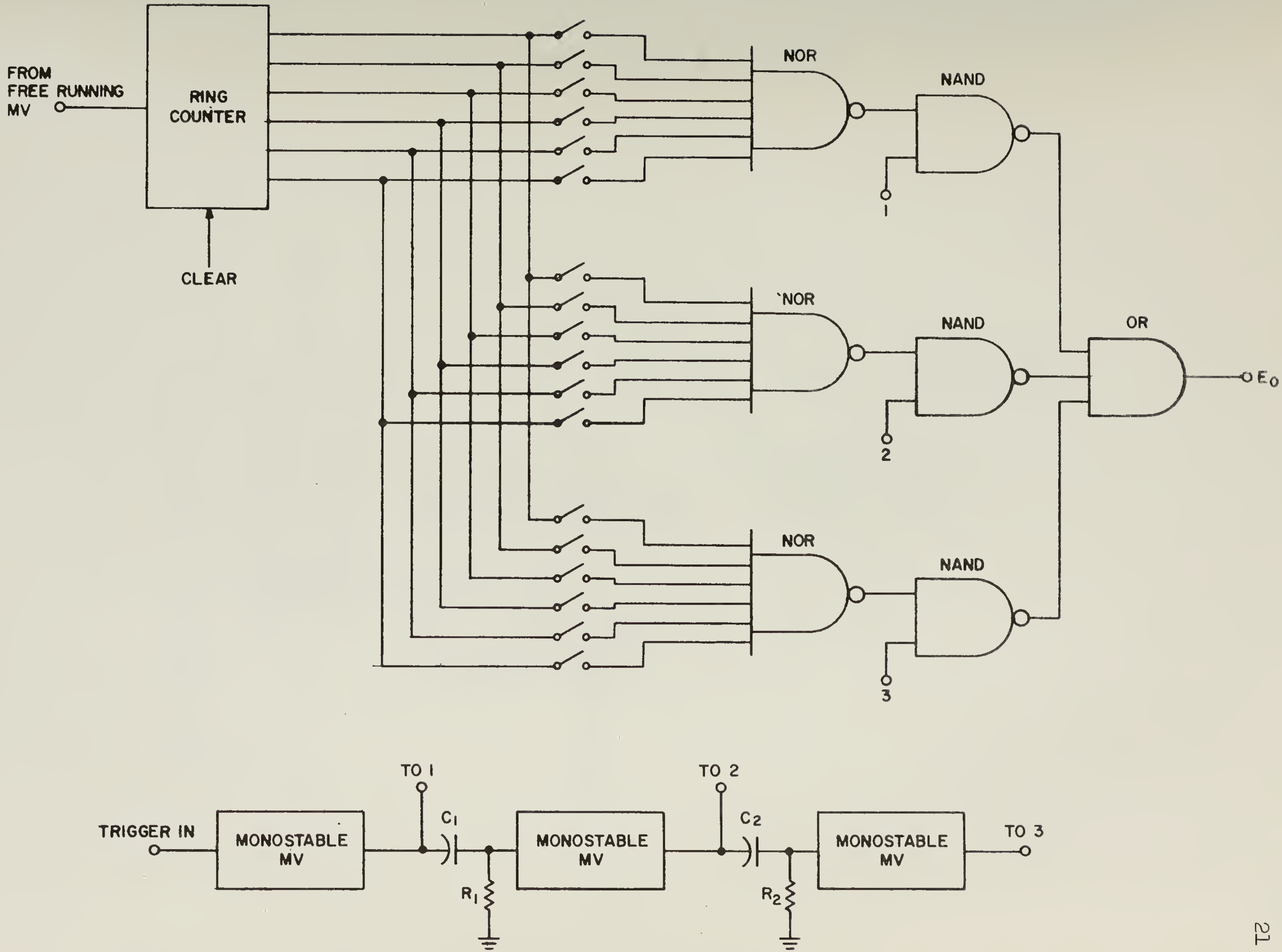

Figure 11. The Multiple Coded Attributes Encoder.

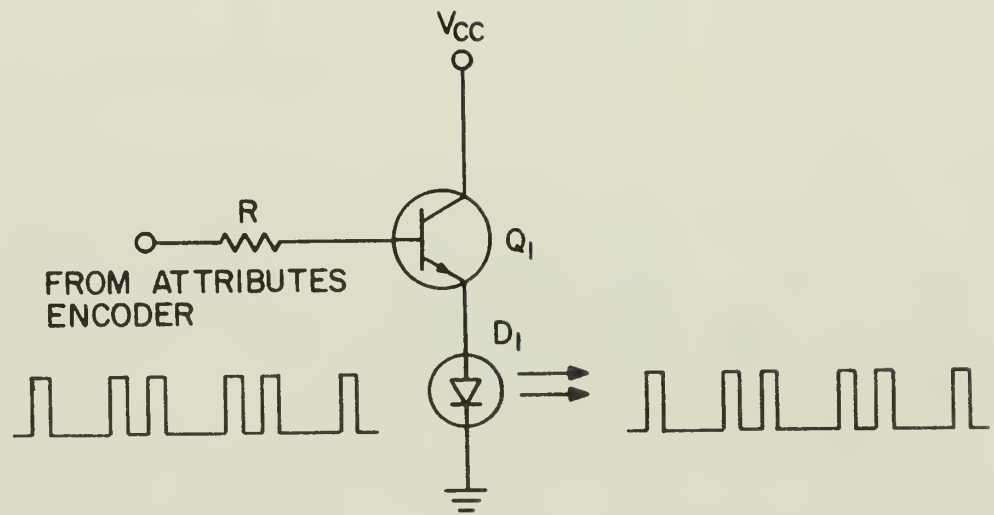

Figure 12. The Infrared Transmitter.

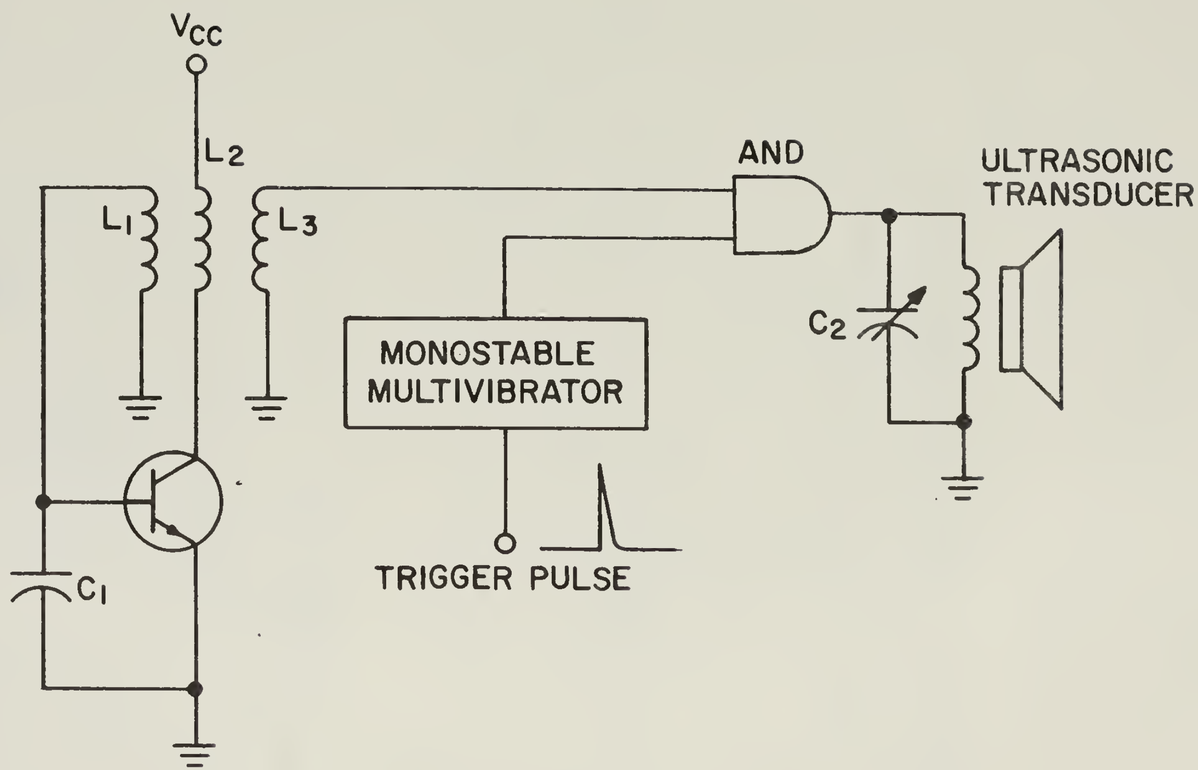

Figure 13. The Locational Marker Generator.

4. THE CIRCUITS AND FUNCTIONS OF THE FRONT END

The front end contains many circuits -- some commonly used circuits and some specially developed circuits. Only the special circuits are described in detail.

4.1 The Ultrasonic Detector and Trigger Circuit

The sensor is a specially designed ultrasonic microphone with low impedance. The output of the sensor is amplified with a high gain integrated circuit amplifier. A Schmitt trigger, consisting of discrete components, is used to generate a pulse when the output of the amplifier reaches a preset level. A simple differential circuit is used to shape the Schmitt trigger output into a sharp pulse. There are four identical detectors for x and y coordinates determination. This circuit is shown in Figure 14.

4.2 The Time Detector

The time detector is simply a flip-flop circuit. Any available IC flip-flop on the market can serve the purpose. A non-inverting buffer circuit is added to the output of the flip-flop. The clock pulse provides a "1" at the output. The pulse from the ultrasonic detector turns it to "0". Thus the pulse width represents the time for the ultrasonic signal to travel from its transducer on the block to the receiver on the front end, plus some propagation delay of the circuit components. The time detector is shown in Figure 15.

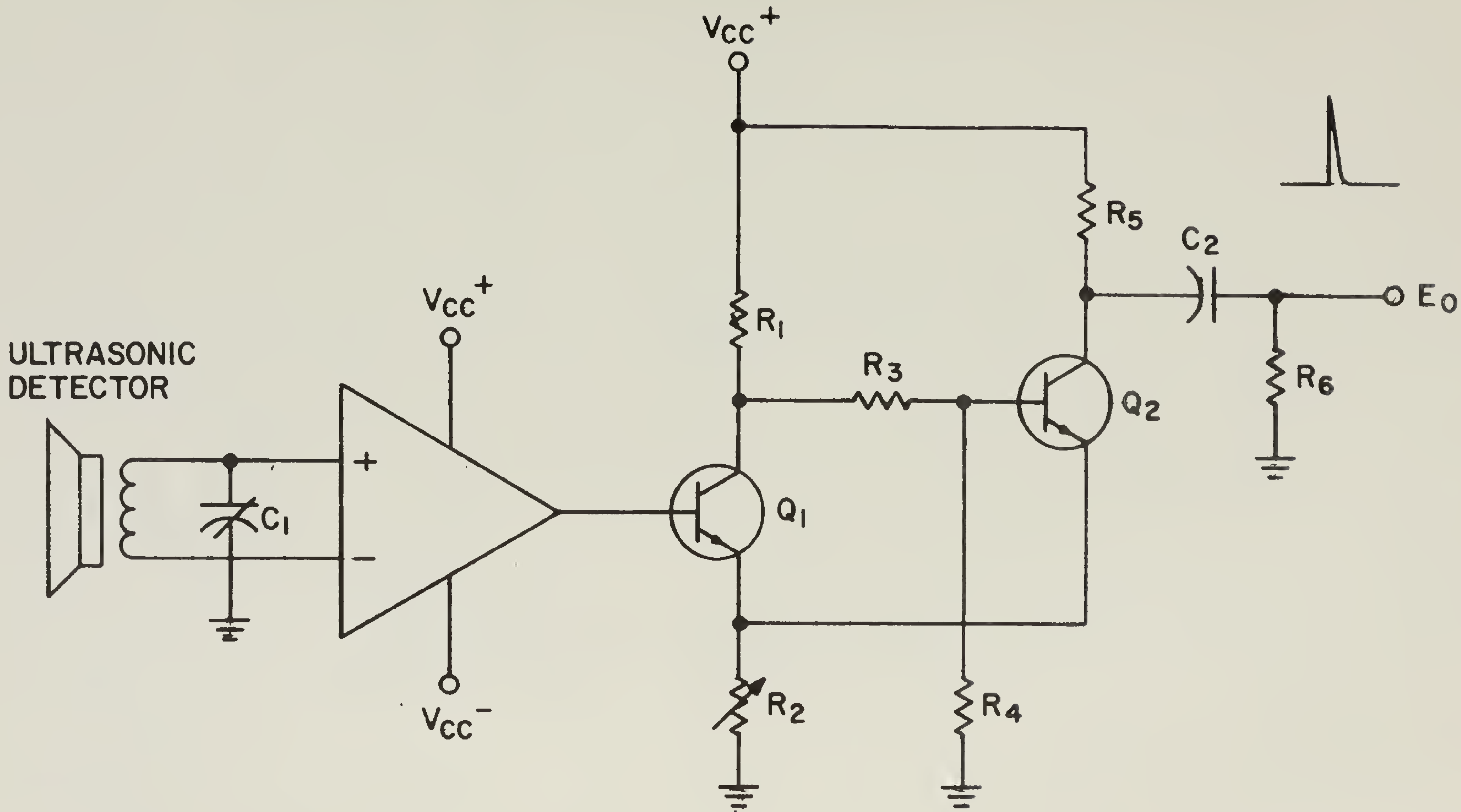

Figure 14. The Locational Marker Detector and Trigger Generator.

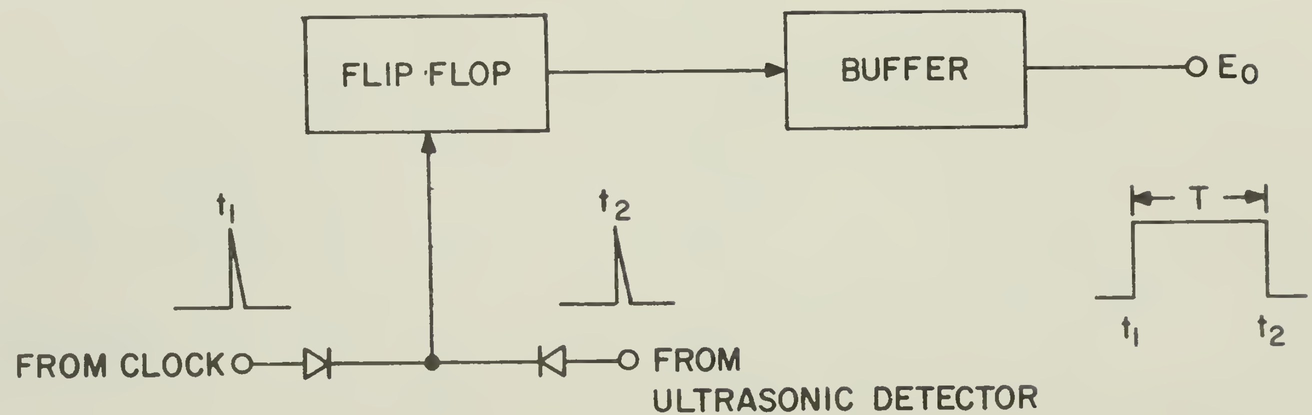

Figure 15. The Time Detector.

4.3 The Serial Number Generator and Transmitter

The generator generates frequencies which represent the serial number of a block. The frequency changes sequentially upon the clock triggering pulse. A BCD counter of 5 bit capacity is used to control high speed reed-relays which change the combination of capacitors to control the oscillation frequency. The frequency range is assumed to be 50 KC - 100 KC with a space of at least 1 KC apart between neighboring signals. Since the counter is a 5 bit BCD counter, a total of 32 serial numbers can be addressed. A monostable multivibrator is used to control the length of the transmission of serial numbers. Figure 16 illustrates the complete circuit diagram of the generator and transmitter. The delay time of the reed relay t_{dr} is measured and used for locational computation. If manual control is desired, the frequency can be controlled by a set of switches.

4.4 The Attributes Detector

The attributes detector is the simplest circuit of all since the signal was coded by the blocks. It is necessary only to detect the coded pulses and restore the signal level. The signal is then stored in a temporary storage register. The circuit is shown in Figure 17.

The IR detector is a bridge circuit. When there is no signal, R_3 is adjusted to null the bridge output. A high gain differential amplifier is used to amplify the signal. A Schmitt trigger restores the logic level and then stores the signal in a register. The attributes signal is coded in 6 bits.

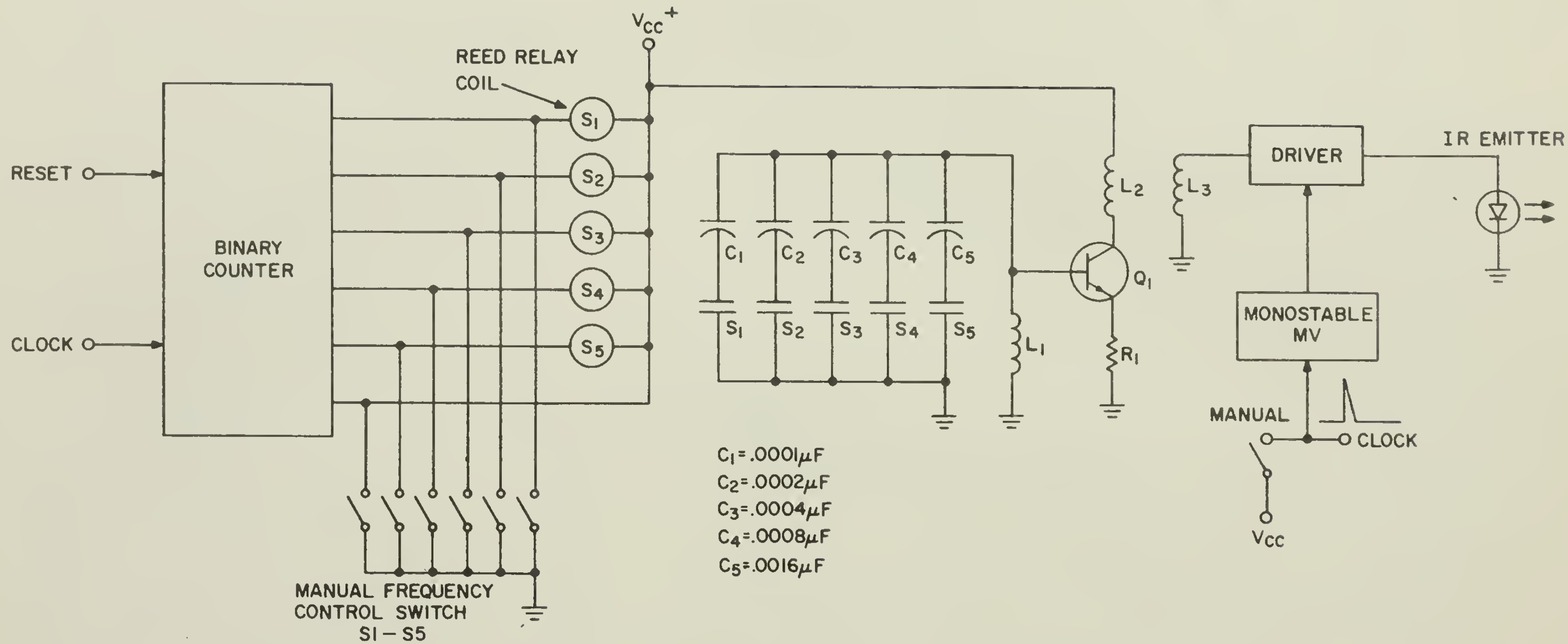

Figure 16. The Serial Number Generator and Transmitter.

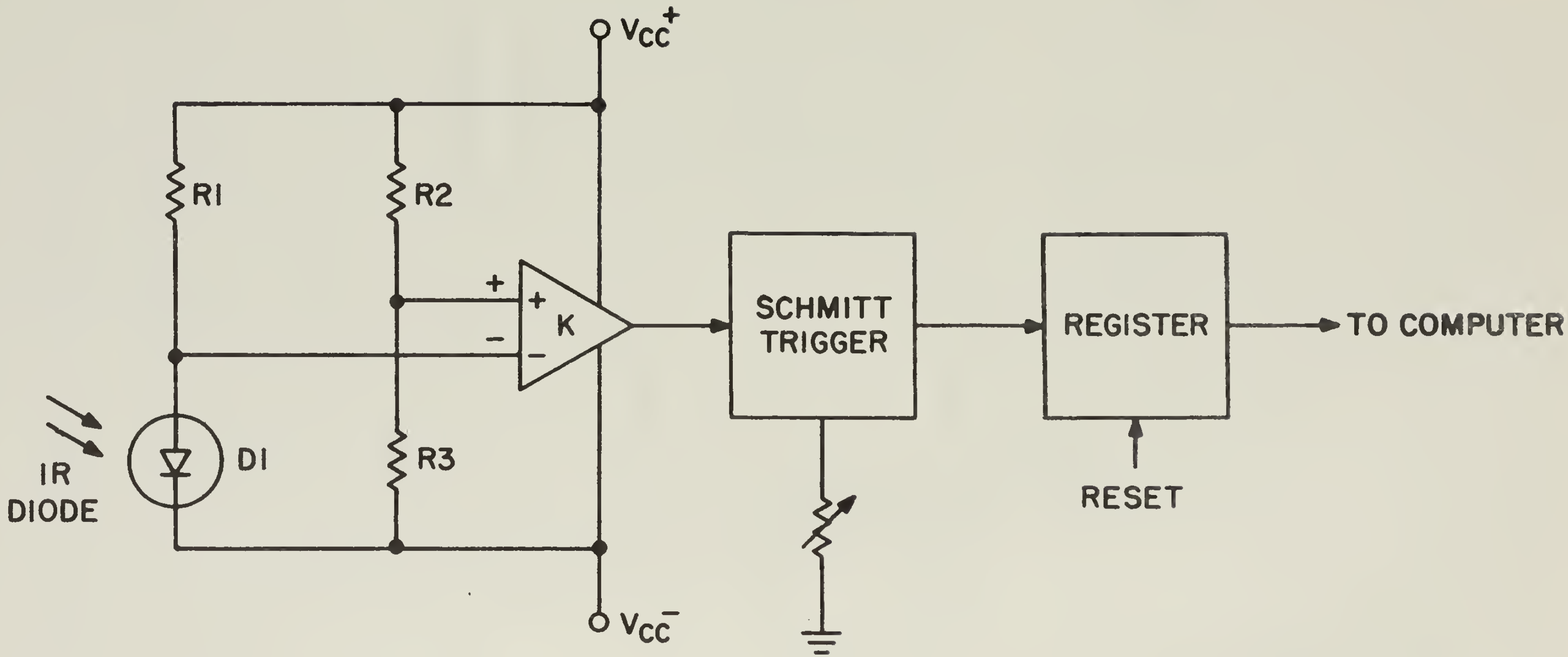

Figure 17. The Attributes Detector.

4.5 The Threshold Detectors (A/D) and Digital Encoders

This is the locational computation output section which converts the analog coordinator information in voltage level to digital form so that the location P(x,y) can be read as $P_i(0,4)$ or $P_j(12,17)$, etc. A basic threshold detector circuit is shown in Figure 18a. The characteristics of the circuit are shown in Figure 18b. A more sophisticated version is shown in Figures 19a and 19b. The overall detection and encoder circuit is shown in Figures 20a and 20b.

4.6 Pulse Time to Voltage Converters

To compute the location of the block, distances in between the block and ultrasonic microphones are measured by the propagation time T_n of the ultrasonic signal. T_n needs to be converted to voltage for analog computation. To convert the pulse time into voltage signal an integrator is used to generate the ramp voltage. The output of the ramp is determined by the two pulses which mark the time T. Figure 21a illustrates the converter. Figure 21b is the characteristics of the time to voltage converter. Figure 22 shows the circuit of a ramp generator.

The working principle of the T to V converter is as follows: The clock pulse triggers the time detector and generates a pulse T. T, together with a positive source, then turns on the ramp generator. Thus, the ramp function is started by the rise of pulse T. When T falls, the ramp function stops rising and a holding circuit arrangement, implemented in the integrator, will hold the peak ramp for many milliseconds to enable the computing of all converted voltages at the same instant. An electronic switch is used to discharge the capacitor of the integrator.

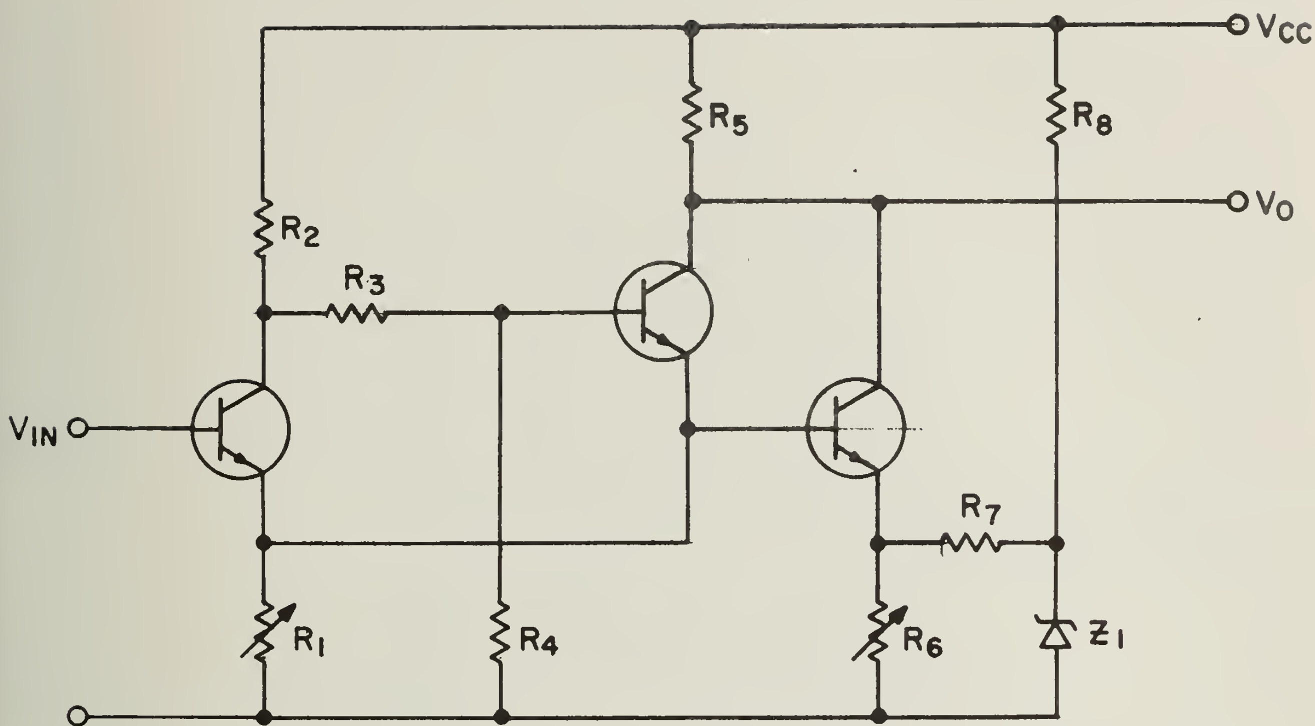

Figure 18a. A Basic Threshold Detector Circuit.

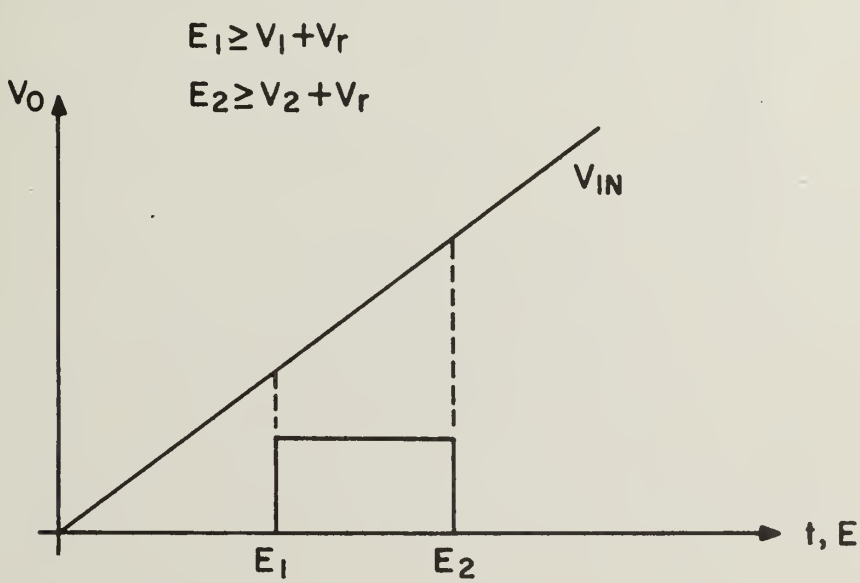

Figure 18b. The Threshold Detector Characteristics.

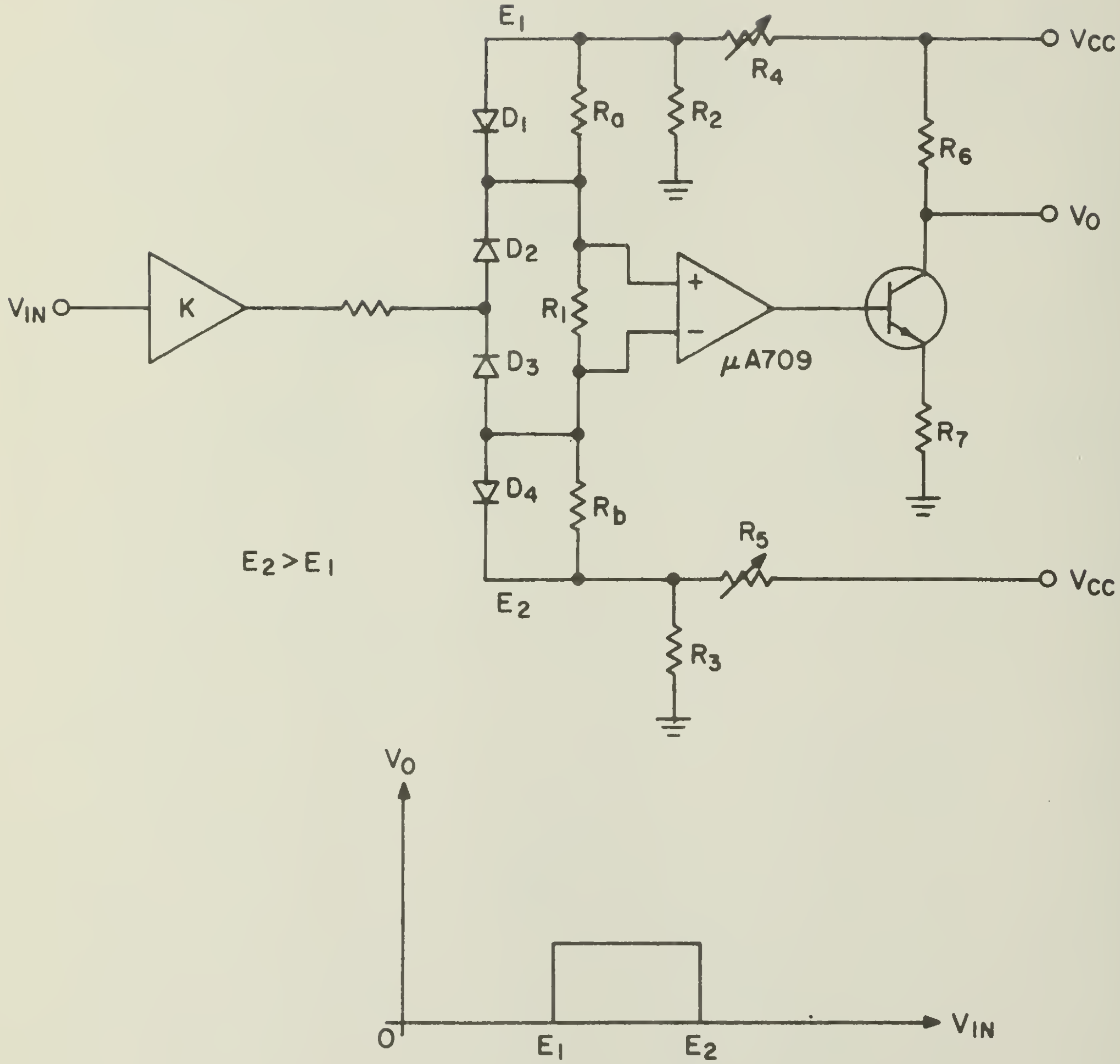

Figure 19a. A Voltage Band Detector Circuit.

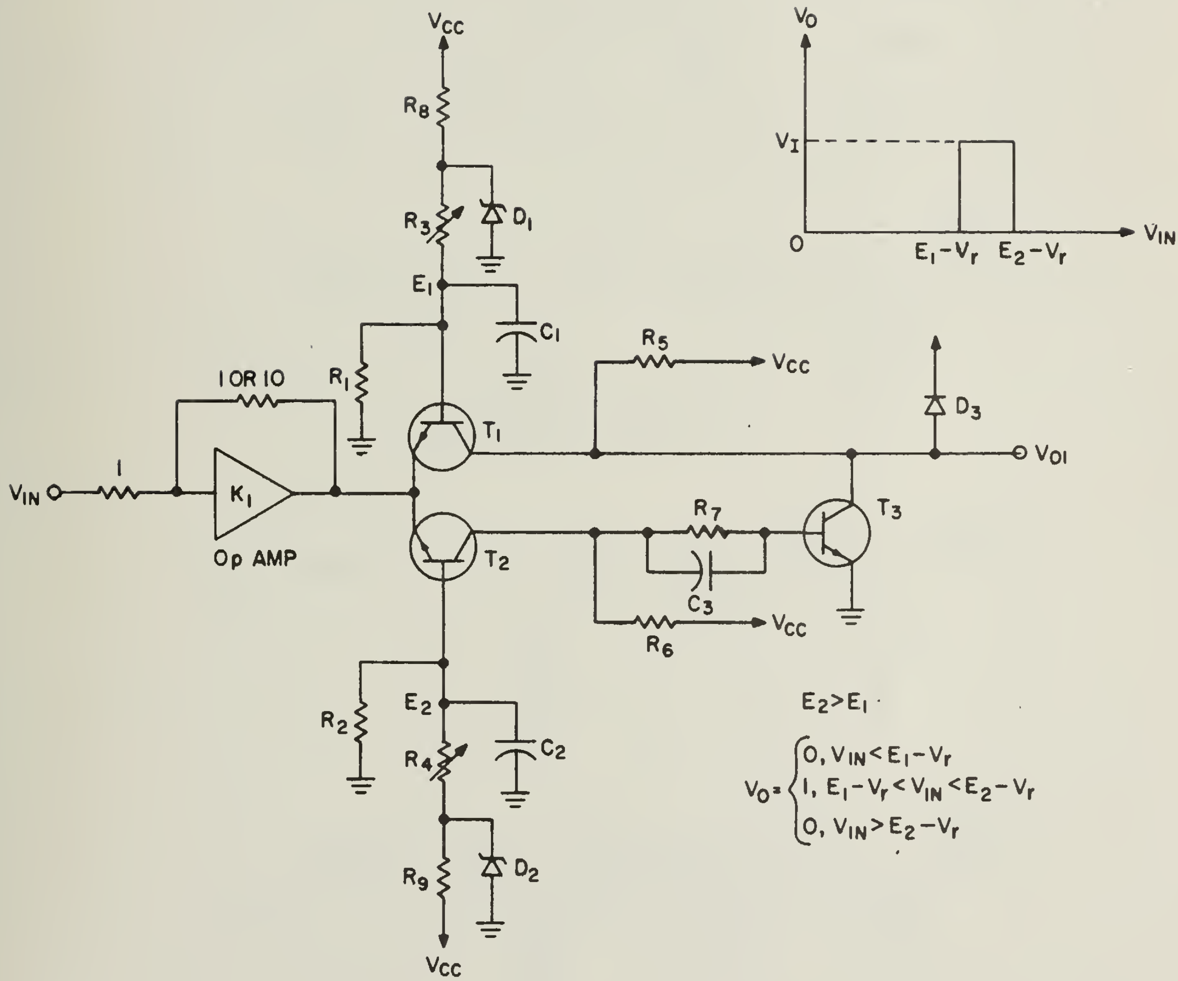

Figure 19b. A Version of a Voltage Band Detector Circuit.

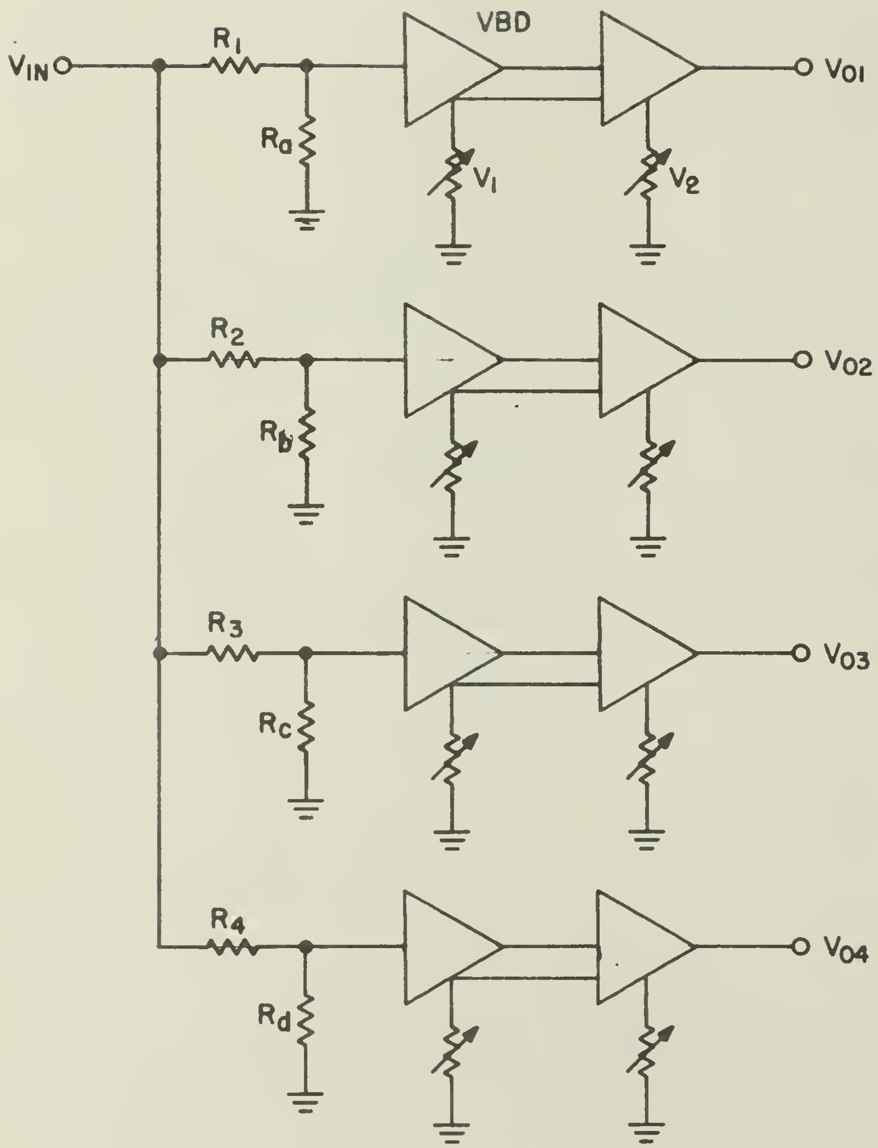

Figure 20a. Threshold Detector and Encoder.

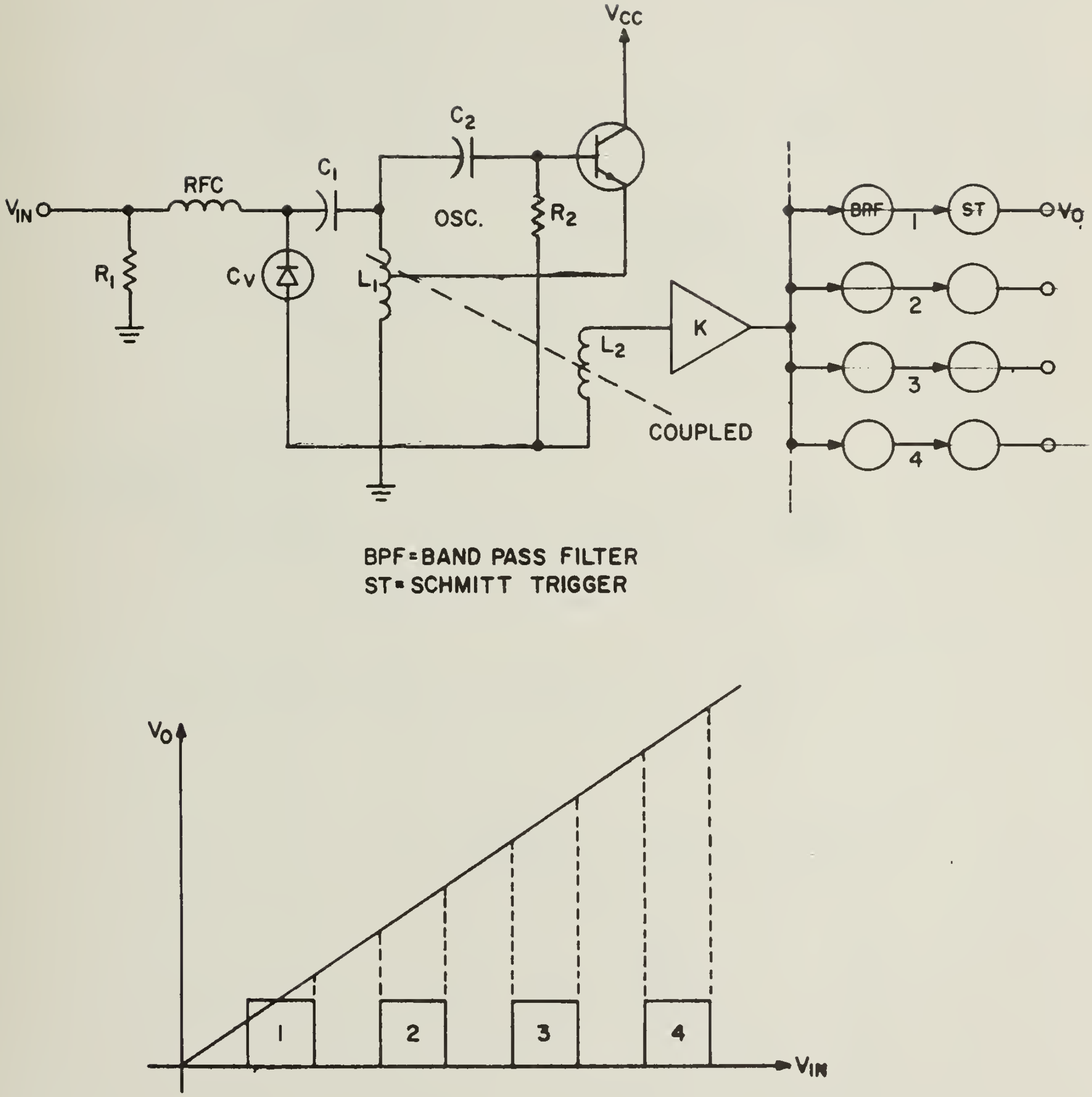

Figure 20b. A Version of a Threshold Detector and Encoder.

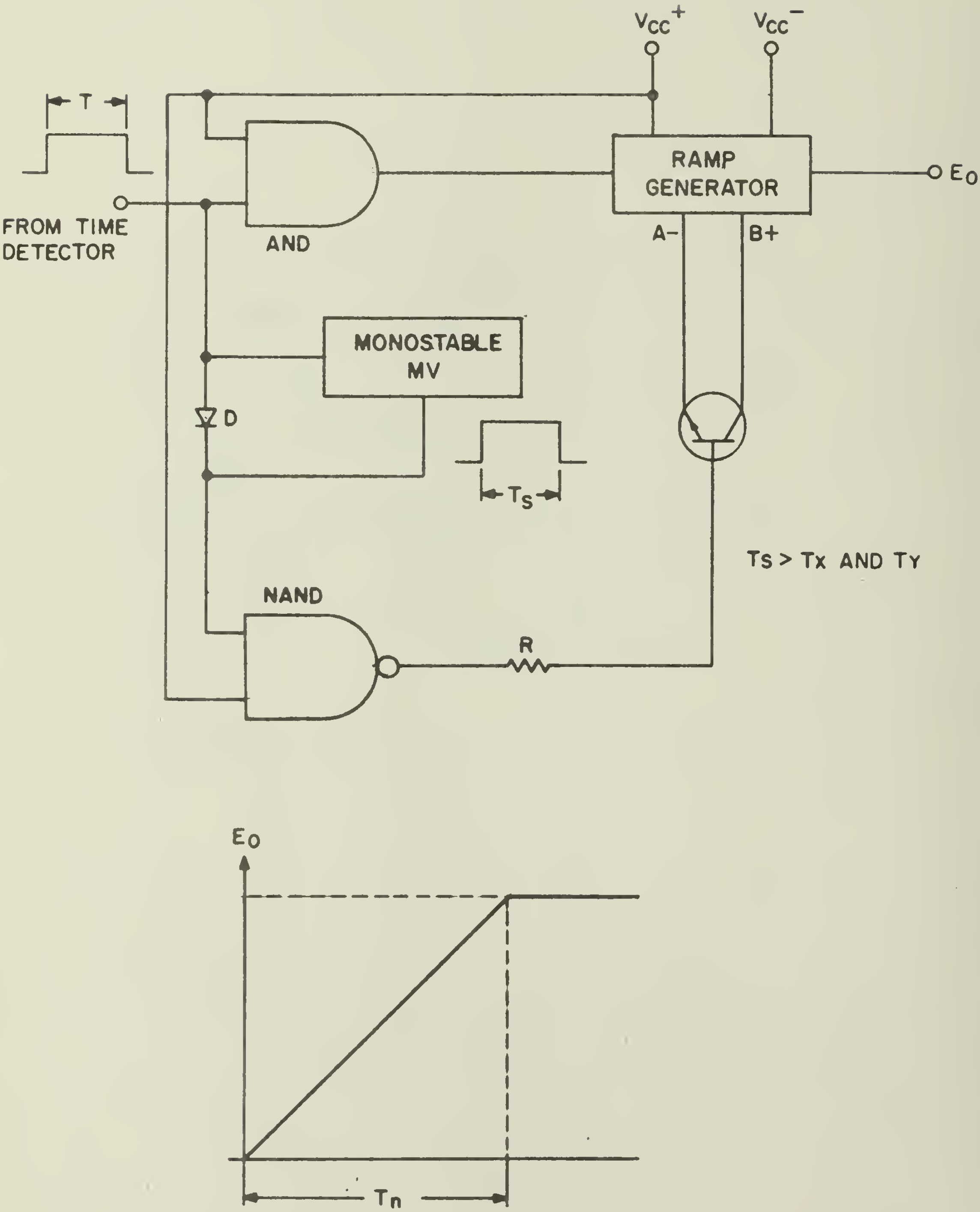

Figure 21. The Time to Voltage Converter and the Characteristics.

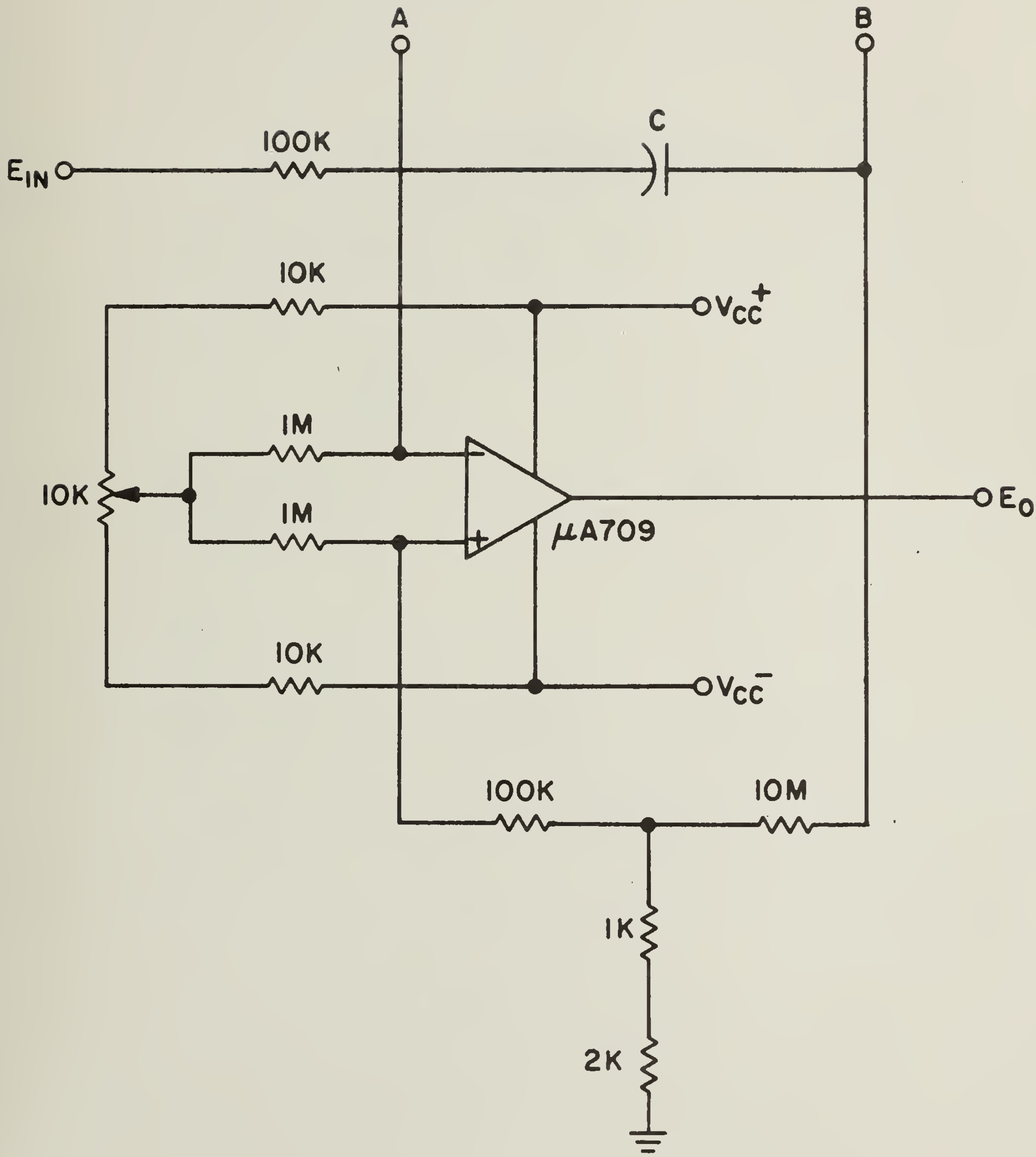

Figure 22. The Ramp Generator and Holder.

The switch is controlled by a monostable multivibrator for the open time (it is a normally closed switch.) There are four identical units like this for the conversion of T_{x1}, T_{x2}, T_{y1} and T_{y2} to V_{x1}, V_{x2}, V_{y1} and V_{y2}.

4.7 <u>The Locational Coordinate Computing Circuit</u>

There are two sets of the computing circuit, one for the x-axis and the other one for the y-axis. This is an analog system which utilizes the availability of integrated circuit analog multipliers and operational amplifiers. To show the computation process, the algorithm which leads to the circuit design is as follows: Let the blocks be placed in an area W x W and enclosed by a wall. The four ultrasonic detectors are mounted on each wall and at the center of the walls. See Figure 23 for the arrangement.

Assume a block B_i is located at point $P_i(x,y)$ and is transmitting the ultrasonic marker. The time for the ultrasonic wave to travel from the block to the detectors DX_1, DX_2, DY_1 and DY_2 are taken to be T_{x1}, T_{x2}, T_{y1} and T_{y2}. The x coordinate and y coordinate can be evaluated with the same arrangement. Figure 24 shows the determination of x.

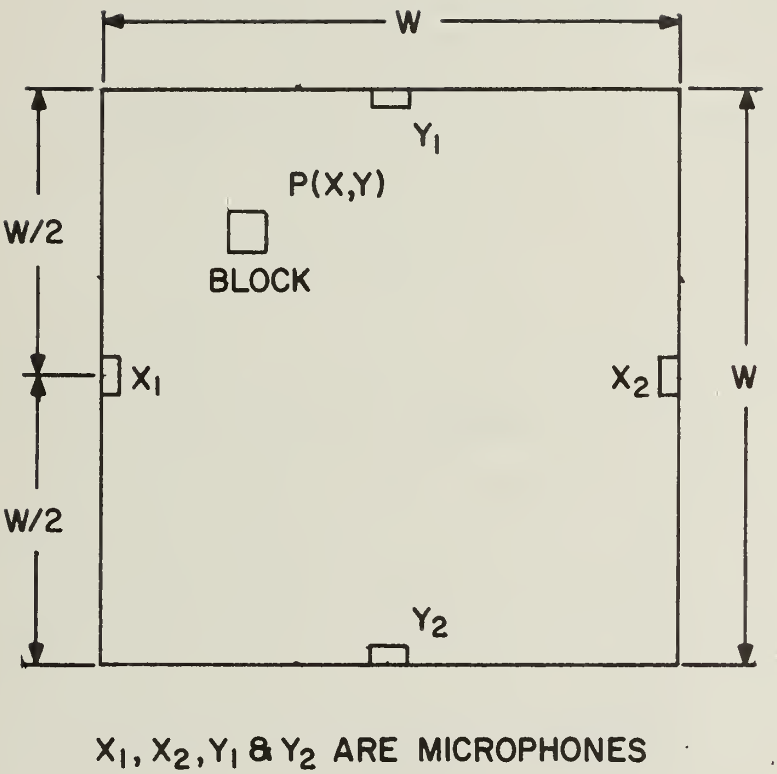

Figure 23. The Location Detection Arrangement.

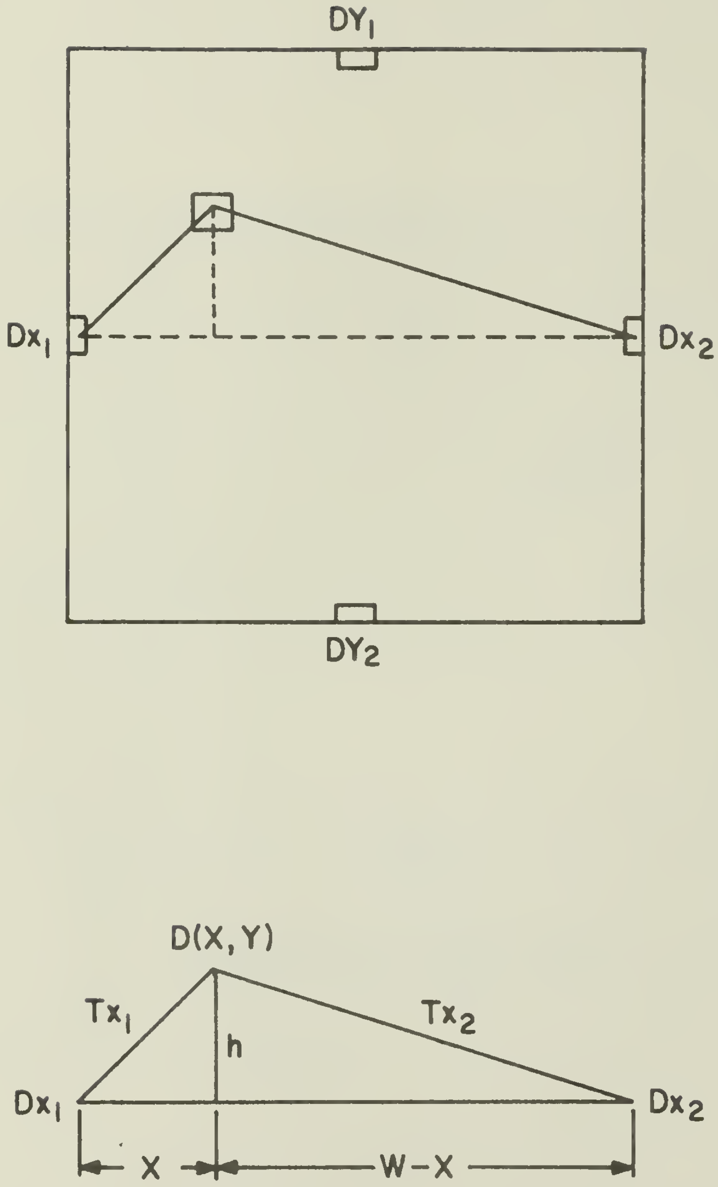

Figure 24. The Determination of x.

It is clear from Figure 24 that x can be found as follows:

$$h^2 = T_{x1}^{\ 2} - x^2 = T_{x2}^{\ 2} - (W-X)^2$$

$$x^2 = T_{x1}^{\ 2} - T_{x2}^{\ 2} - W^2 + 2WX + x^2$$

$$\therefore\ x = \frac{T_{y1}^{\ 2} - T_{x2}^{\ 2} + W^2}{2W}$$

y can be found with the same manner as

$$y = \frac{T_{y1}^{\ 2} - T_{y2}^{\ 2} + W^2}{2W}$$

The computing circuit is shown in Figure 25.

In order to do the computation after V_{x1} and V_{x2} are all obtained before the multiplier is operating, a control circuit is designed by using a monostable multivibrator which starts a pulse M by the main clock pulse and ends at $t = T_x max$. The multiplier operates at the end of the pulse M. The output V_0 is then coded into digital form.

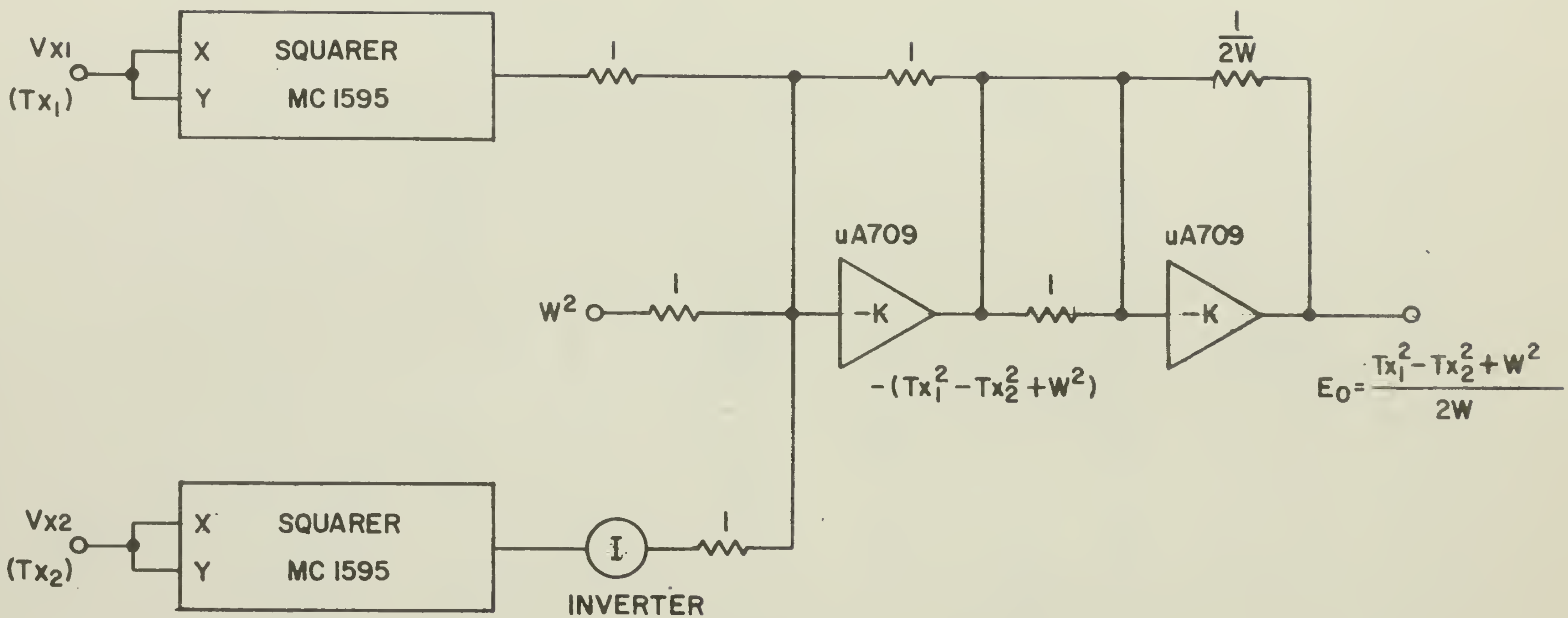

Figure 25. The Analog Computing Circuit.

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